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CHAPTER II

Preliminary Classification:

Proposed Class:

Subclass:

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(ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

PCT/DE99/03961	08 December 1999 (8.12.99)	14 December 1998 (14.12.98)
International Application Number	**International Filing Date**	**International Earliest Priority Date**

TITLE OF INVENTION: BIPOLAR TRANSISTOR AND METHOD FOR PRODUCING SAME

APPLICANT(S): INSTITUT FUER HALBLEITERPHYSIK FRANKFURT (ODER) GmbH; HEINEMANN, Dr. Bernd; EHWALD, Karl-Ernst and KNOLL, Dr. Dieter

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CERTIFICATION UNDER 37 C.F.R. SECTION 1.10*

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ATTENTION: EO/US

1. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. Section 371:

a. This express request to immediately begin national examination procedures (35 U.S.C. Section 371(f)).

b. The U.S. National Fee (35 U.S.C. Section 371(c)(1)) and other fees (37 C.F.R. Section 1.492) as indicated below:

2. Fees

CLAIMS FEE*	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALC-ULATIONS
	TOTAL CLAIMS	11 -20 =	0	x $18.00 =	$0 00
	INDEPEN-DENT CLAIMS	2 - 3 =	0	x $80 00 =	$0 00
	MULTIPLE DEPENDENT CLAIM(S) (if applicable) + $270 00				$270 00
BASIC FEE	U S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in Section 1.482 has been paid to the U.S PTO, and payment of an international search fee as set forth in Section 1 445(a)(2) to the U.S. PTO· where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 C F.R. Section 1 492(a)(5)) $860 00				$860.00
	Total of above Calculations				= $1,130.00
SMALL ENTITY	Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed (note 37 CFR Sections 1 9, 1.27, 1.28)				- $0 00
	Subtotal				$1,130.00
	Total National Fee				$1,130 00
	Fee for recording the enclosed assignment document $40 00 (37 C.F.R Section 1.21(h)) See attached "ASSIGNMENT COVER SHEET".				$0.00
TOTAL	Total Fees enclosed				$1,130.00

DO NOT CHARGE FEE FOR MUJLTIPLE DEPENDENT CLAIMS. A PRELIMINARY AMENDMENT RESOLVING MULTIPLE DEPENDENCY WILL BE FILED WITH THE NECESSARY TRANSLATIONS.

A check in the amount of $860.00 to cover the above fees is enclosed.

3. A copy of the International application as filed (35 U.S.C. Section 371(c)(2)) has been transmitted by the International Bureau.

Date of mailing of the application (from form PCT/IB/308): 22 June 2000

4. A translation of the International application into the English language (35 U.S.C. Section 371(c)(2)) will follow.

5. Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. Section 371(c)(3)) have been transmitted by the International Bureau.

Date of mailing of the amendment (from form PCT/IB/308): not known.

6. A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. Section 371(c)(3)) has not been transmitted.

7. A copy of the international examination report (PCT/IPEA/409) is transmitted herewith.

8. Annex(es) to the international preliminary examination report is/are transmitted herewith.

9. A translation of the annexes to the international preliminary examination report is not transmitted herewith.

10. An oath or declaration of the inventor (35 U.S.C. Section 371(c)(4)) complying with 35 U.S.C. Section 115 is submitted herewith, and such oath or declaration identifies the application and any amendments under PCT Article 19 that were transmitted as stated in Section 3 and/or 5; and states that they were reviewed by the inventor as required by 37 C.F.R. Section 1.70. The declaration has not been signed by the applicants.

II. Other document(s) or information included:

11. An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a) has been transmitted by the International Bureau.

Date of mailing (from form PCT/IB/308): 26 April 2000.

12. An Information Disclosure Statement under 37 C.F.R. Sections 1.97 and 1.98 will be transmitted within THREE MONTHS of the date of submission of requirements under 35 U.S.C. Section 371(c).

13. Additional documents:

a. Copy of request (PCT/RO/101)

b. International Publication No. WO00/36653
Front page only

14. The above items are being transmitted before 30 months from any claimed priority date.

AUTHORIZATION TO CHARGE ADDITIONAL FEES

The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to Account No.: 15-0450

37 C.F.R. Section 1.492(a)(1), (2), (3), and (4) (filing fees)

Date: 11 June 2001

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Heinemann, et al.	Examiner:	Unknown
Ser. No.:	09/857,857	Art Group:	Unknown
Title:	BIPOLAR TRANSISTOR AND METHOD FOR PRODUCING SAME		
Filed:	11 June 2001	Date:	23 August 2001

PRELIMINARY AMENDMENT

This Preliminary Amendment is filed with the completion of the filing requirements in this case, which is a national stage entry of PCT case DE99/03961, which in turn claims priority from an application filed in Germany as 198 57 640.4 on 14 December 1998. The fees for the claims should be calculated based on the claims remaining after the entry of this Preliminary Amendment, which results in 14 total and 4 independent claims. Consistent with the modifications to 37 CFR §1.121, the applicant has provided the amended claims in a clean form on the attached sheets.

Amendments to the Disclosure

The specification as filed has been altered from the literal translation document received to delete information above the title, to insert headings according to US practice, and to insert paragraph numbering in lieu of line numbering, but no amendments are made to the content. That copy of the specification should be used for examination.

Amendments to the Figures

None at this time.

Amendments to the Abstract:

None at this time

Amendments to the Claims

Please amend the claims as follows:

1. (amended) A procedure for the manufacture of a bi-polar transistor, during which structured regions consisting of a collector region [(112)] and an insulation region that [(113) - which] surrounds the collector region [(112) -] are produced on a monocrystal substrate layer [(111)], a base layer [(115)] and, by means of epitaxy, a cap layer [(116)] are produced over the

collector region [zone (112) –] where an interposed buffer layer [(114)] can be deposited [-], an insulation layer [(117)] is deposited over the cap layer [(116)], the insulation layer [(117)] is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer [(117)] and is then used as an emitter-doping agent source and as a contact layer, wherein, [characterized in that –] before the diffusion from the emitter-doping agent source, [-] a doping profile is introduced into the cap layer [(116)], and the profile is low-doped on the base side and highly doped on the emitter side.

2. (amended) The [A] procedure according to claim 1, wherein [characterized in that] the base-side lower doping concentration of the cap layer [(116)] does not exceed values of 5×10^{16} cm^{-3}.

3. (amended) The [A] procedure of claim 1, wherein [according to claims 1 or 2, characterized in that] the cap layer [(116)] is of a thickness between 20 nm and 70 nm.

4. (amended) The [A] procedure of claim 1, wherein [according to one or several of the preceding claims, characterized in that] the emitter-side high doping concentration of the cap layer [(116)] does not exceed values of 5×10^{18} cm^{-3} when [if] the doping agent is of the same conductivity type as the base layer [(115)].

5. (amended) The [A] procedure of claim 1, wherein [according to one or several of the preceding claims, characterized in that] the cap doping profile is introduced by implantation.

6. (amended) The [A] procedure of claim 1, wherein [according to one or several of the preceding claims, characterized in that] the cap doping profile is introduced in situ during the epitaxy process.

7. (amended) The [A] procedure of claim 1, wherein [according to one or several of the preceding claims, characterized in that] the cap doping profile is introduced by diffusion from the insulation layer [(117)] after highly enriching the insulation layer [that had been highly enriched] with the doping agent.

8. (amended) A bi-polar transistor, in which structured regions consisting of a collector region [(112)] and an insulation region that [(113) - which] surrounds the collector region [(112) -] are produced on a monocrystal substrate layer [(111)], a base layer [(115)] and , [–] where a buffer layer [(114)] can be interposed [-], by means of epitaxy, a cap layer [(116)] are produced over the collector zone [(112)], an insulation layer [(117)] is deposited over the cap layer [(116)], the insulation layer [(117)] is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer [(117)] and is then used as an emitter-doping agent source and as a contact layer, wherein [characterized in that], in an [the] overlapping region [(17) – the region] between an [the] edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer [(15) –] the cap layer [(13/116)] contains a doping profile, and the profile is low-doped on the base side and highly doped on the emitter side.

9. (amended) The [A] bi-polar transistor according to claim 8, wherein [characterized in that] the base-side lower doping concentration of the cap layer [(13/116)] does not exceed values of 5×10^{16} cm^{-3}.

10. (amended) The [A] bi-polar transistor of Claim 8, wherein [according to one or several of claims 8 to 9, characterized in that] the cap layer [(13/116)] is of a thickness between 20 nm and 70 nm.

11. (amended) The [A] bi-polar transistor of Claim 8, wherein [according to one or several of claims 8 to 10, characterized in that] the emitter-side high doping concentration of the cap layer [(13/116)] does not exceed values of 5×10^{18} cm^{-3} when [if] the doping agent is of the same conductivity type as the base layer [(12,115)].

12. (new) A procedure for manufacturing a bi-polar transistor, comprising the steps of:

producing, on a monocrystal substrate layer, structured regions consisting of a collector region and an insulation region, the insulation region surrounding the collector region,

producing a base layer and a cap layer over the collector region, the cap layer produced by epitaxy;

depositing an insulation layer over the cap layer, the insulation layer opened in an area of an effective emitter zone; and

depositing and structuring a poly-Si or an α-Si layer over the opened insulation layer, and using this layer as a source of emitter-doping agent and as a contact layer;

wherein, before diffusing from the emitting-doping agent source, a doping profile is introduced into the cap layer, the profile being low doped on a base side thereof and high doped on an emitter side thereof.

13. (new) The procedure of claim 12, further comprising the step of depositing a buffer layer between the collector region and the base layer.

14. (new) A bi-polar transistor, comprising:

a monocrystal substrate layer;

structured regions comprising a collector region and an insulation region surrounding the collector region atop the monocrystal substrate layer;

a base layer and, by means of epitaxy, a cap layer produced over the collector region when a buffer layer can be interposed;

an insulation layer deposited over the cap layer, the insulation layer being opened in an area of an effective emitter zone; and

a poly-Si or an α-Si layer deposited and structured over the opened insulation layer, this layer then used as an emitter-doping agent source and as a contact layer,

wherein, in an overlapping region between an edge of the emitter zone and an outer delimitation of the structured poly-silicon or α-silicon layer, the cap layer contains a doping profile, and the profile is low-doped on a base side thereof and highly doped on an emitter side thereof.

REMARKS

The above claims have been amended to more closely correspond them to United States claiming practice, namely, by removing multiple dependencies, especially improper multiple dependencies, by removing reference numerals, and by clarifying antecedent basis issues. These amendments to the claims are fully supported by the literal translation into English of the specification as filed in Germany, and they do not introduce new subject matter. Further, these amendments to the claims are not narrowing in scope.

The claims as amended are provided on clean sheets.

Respectfully submitted,

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CLAIMS AS AMENDED

1. (amended) A procedure for the manufacture of a bi-polar transistor, during which structured regions consisting of a collector region and an insulation region that surrounds the collector region are produced on a monocrystal substrate layer, a base layer and, by means of epitaxy, a cap layer are produced over the collector region where an interposed buffer layer can be deposited, an insulation layer is deposited over the cap layer, the insulation layer is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer and is then used as an emitter-doping agent source and as a contact layer, wherein, before the diffusion from the emitter-doping agent source, a doping profile is introduced into the cap layer, and the profile is low-doped on the base side and highly doped on the emitter side.

2. (amended) The procedure according to claim 1, wherein the base-side lower doping concentration of the cap layer does not exceed values of 5×10^{16} cm^{-3}.

3. (amended) The procedure of claim 1, wherein the cap layer is of a thickness between 20 nm and 70 nm.

4. (amended) The procedure of claim 1, wherein the emitter-side high doping concentration of the cap layer does not exceed values of 5×10^{18} cm^{-3} when the doping agent is of the same conductivity type as the base layer.

5. (amended) The procedure of claim 1, wherein the cap doping profile is introduced by implantation.

6. (amended) The procedure of claim 1, wherein the cap doping profile is introduced in situ during the epitaxy process.

7. (amended) The procedure of claim 1, wherein the cap doping profile is introduced by diffusion from the insulation layer after highly enriching the insulation layer with the doping agent.

8. (amended) A bi-polar transistor, in which structured regions consisting of a collector region and an insulation region that surrounds the collector region are produced on a monocrystal substrate layer, a base layer and , where a buffer layer can be interposed, by means of epitaxy, a cap layer are produced over the collector zone, an insulation layer is deposited over the cap layer, the insulation layer is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer and is then used as an emitter-doping agent source and as a contact layer,

wherein, in an overlapping region between an edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer the cap layer contains a doping profile, and the profile is low-doped on the base side and highly doped on the emitter side.

9. (amended) The bi-polar transistor according to claim 8, wherein the base-side lower doping concentration of the cap layer does not exceed values of 5×10^{16} cm^{-3}.

10. (amended) The bi-polar transistor of Claim 8, wherein the cap layer is of a thickness between 20 nm and 70 nm.

11. (amended) The bi-polar transistor of Claim 8, wherein the emitter-side high doping concentration of the cap layer does not exceed values of 5×10^{18} cm^{-3} when the doping agent is of the same conductivity type as the base layer.

12. (new) A procedure for manufacturing a bi-polar transistor, comprising the steps of:

producing, on a monocrystal substrate layer, structured regions consisting of a collector region and an insulation region, the insulation region surrounding the collector region,

producing a base layer and a cap layer over the collector region, the cap layer produced by epitaxy;

depositing an insulation layer over the cap layer, the insulation layer opened in an area of an effective emitter zone; and

depositing and structuring a poly-Si or an α-Si layer over the opened insulation layer, and using this layer as a source of emitter-doping agent and as a contact layer;

wherein, before diffusing from the emitting-doping agent source, a doping profile is introduced into the cap layer, the profile being low doped on a base side thereof and high doped on an emitter side thereof.

13. (new) The procedure of claim 12, further comprising the step of depositing a buffer layer between the collector region and the base layer.

14. (new) A bi-polar transistor, comprising:

a monocrystal substrate layer;

structured regions comprising a collector region and an insulation region surrounding the collector region atop the monocrystal substrate layer;

a base layer and, by means of epitaxy, a cap layer produced over the collector region when a buffer layer can be interposed;

an insulation layer deposited over the cap layer, the insulation layer being opened in an area of an effective emitter zone; and

a poly-Si or an α-Si layer deposited and structured over the opened insulation layer, this layer then used as an emitter-doping agent source and as a contact layer,

wherein, in an overlapping region between an edge of the emitter zone and an outer delimitation of the structured poly-silicon or α-silicon layer, the cap layer contains a doping profile, and the profile is low-doped on a base side thereof and highly doped on an emitter side thereof.

BI-POLAR TRANSISTOR AND A PROCEDURE FOR ITS MANUFACTURE

[0001] The invention relates to a bi-polar transistor and a procedure for its manufacture.

BACKGROUND OF THE ART

[0002] The implementation of epitaxially manufactured silicon-germanium hetero-bi-polar transistors (SiGe HBT) and the resulting cost-reducing simplification of the technological processes have lately provided a new impetus for a further development of Si bi-polar transistors. In this respect, the combination of an epitaxially produced base with the process-simplifying possibilities of the single polysilicon technology offers an attractive direction of development.

[0003] In comparison with conventional base profiles produced by implantation or diffusion, silicon-germanium base layers made by epitaxy allow producing, simultaneously, smaller base widths and base layer resistance without unusable small current gains or high leakage currents. The technology allows implementation of a concentration of the active doping agent of up to 1 x 10^{20} cm^{-3}, as is described – for example – in *A. Schüppen, A. Gruhle, U. Erben, H. Kibbel und U. König: 90 GHz fmax SiGe-HBTs, DRC 94*, page IIA-2, 1994. However, in order to prevent leakage currents due to tunnel processes, a low-doped region is required between the high-concentration zones of the emitter and the base. As a matter of fact, if the base doping exceeds the value of 5 x 10^{18} cm^{-3}, and if the high concentration of the emitter reaches down to the base – as is usual with implanted base profiles – the consequence is the existence of unacceptably high tunnel currents. As opposed to implanted base profiles, the application of epitaxy allows, simultaneously and without any problems, the production of narrow base profiles and a low-doped region (cap layer).

[0004] Figure 1 illustrates the emitter zone of a SiGe HBT. This transistor design reflects typical characteristics of a single poly-silicon process. An SiGe base 12 and subsequently a cap layer 13 were deposited over a monocrystal collector zone 11. Figure 1 does not show a lateral insulation of the transistor zone. If semiconductor material grows both on the monocrystal substrate 11 and on the insulator zone – not shown in the picture – (i.e., differential epitaxy), it is possible to utilize the grown semiconductor layers as a connection between a contact on the insulation zone and the inner transistor. Such a connection should be designed with as low impedance as possible. This is why it would be advantageous if the

epitaxial layer thickness could be set up independently from the base width. A poly-silicon or an α-silicon layer 15 is deposited on an insulation layer 14, in which emitter windows were etched by means of a wet-chemical etching process. During the deposition or subsequently, the α-silicon layer 15 obtains – by implantation – a doping of the emitter's conductivity type and serves as diffusion source for the emitter doping 16 in the monocrystal substrate. Insulator layer 14 is applied in order to prevent damage to cap layer 13 during the structuring of the polycrystal α-silicon layer 15 performed later. In the overlapping region 17 – a zone between the edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer 15, a layer sequence arises consisting of semiconductor material, insulator material and semiconductor material. Depending on the doping of the cap layer 13, the interfacial charges and the recombination properties of the surface as well as on the operation conditions of the transistor, this design can cause – analogous to a MOS capacity – an enhancement but also a depletion of mobile charge carriers on the surface of the cap layer 13. With a forward-current base-emitter diode, this can affect both the ideal nature of the base current and the low-frequency noise properties. Under certain circumstances, generation currents and breakdown voltage in the non-conducting direction can be affected. The condition that – due to the tunnel (currents) danger – the doping agent concentration should not exceed the value of 5×10^{18} cm^{-3} leads to the question, by means of which procedure this zone should be suitably doped. The following text discusses the variants for SiGe HBT so far known: homogeneous n-doping or p-doping near the tunnel limit or quasi undoped zones (i-zones). *A. Chantre, M. Marty, J.L. Regolini, M. Mouis, J. de Pontcharra, D. Dutrtre, C. Morin, D. Gloria, S. Jouan, R. Pantel, M. Laurens and A. Monroy: A high performance low complexity SiGe HBT for BiCMOS integration, BCTM '98, 1998*, pages 93 – 96 uses a p-doping of about 5×10^{18} cm^{-3}. This results in a decisive disadvantage in that the thickness of the cap layer must be set up within a tolerance range of a few nanometers from the penetration depth of the doping agent diffusing from the poly-silicon emitter layer. Greater cap layer thickness values (which would be advantageous for a low-impedance connection between the inner base and a connector in the insulation zone) are not possible since it would negatively affect the effect of the germanium profile. *A. Gruhle, C. Mähner: Low l/f noise SiGe HBTs with application to low phase noise microwave oscillators, Electronics Letters, Vol. 33, No. 24, 1997*, pages 2050 – 2052 uses a cap layer 100 nm thick with an n-concentration of $1 - 2 \times 10^{18}$ cm^{-3}. EP-A-0 795 899 indicates similar conditions, where preferably a cap layer of a thickness of 70 nm with a n-doping concentration of 2×10^{18} cm^{-3}

is used. Although this variant eliminates the problem of the thickness tolerance, and avoids the danger of tunnel currents by reducing the doping agent concentration in the cap layer, it still does not take full advantage of the possibilities of reducing the base-emitter capacity.

[0005] This disadvantage can be eliminated by not doping the cap layer as is described, for example, in *B. Heinemann, F. Herzel and U. Zillmann: Influence of low doped emitter and collector regions on high-frequency performance SiGe-base HBTs, Solid-St. Electron, 1995*, Volume 38(6), pages 1183 - 1189. However, it can easily lead to a depletion of the aforementioned overlapping region 17. These connections are explained in further text by means of a two-dimension design element simulation.

[0006] Figure 2 shows the simplified transistor design used in the simulation. The electrical effect of the oxide semiconductor surface in the overlapping region is modeled by means of a positive surface charge density of 1×10^{11} cm^{-2} and a surface recombination speed of 1000 cm/s. Figure 3 illustrates vertical profiles along a section line horizontal to the overlapping region. The profiles show three doping variants in the cap layer 13 and a p-doped SiGe base 12 identical for all three cases. The following cap doping cases are compared: a quasi undoped cap layer 13 (profile i) and two homogeneous n-dopings (profile n1 with 1×10^{18} cm^{-3} and profile n2 with 2×10^{17} cm^{-3}). Figure 4 shows the transition frequency as a function of the collector current for various doping variants. Especially with small collector currents, an increase in transition frequency with a falling doping level in the cap layer 13 can be noticed. While profile i provides relatively best transition frequencies, it has, however, the disadvantage that the ideal nature of the base current (Figure 5) is noticeably affected in comparison with the other profiles.

SUMMARY OF THE INVENTION

[0007] The task of this invention is to indicate a bi-polar transistor and a procedure for its manufacture that eliminates the described disadvantages of conventional arrangements, in order to achieve especially minimal base-emitter capacities and best high-frequency properties without noticeably affecting the static properties of the bi-polar transistor with a low-doped cap layer - above all the ideal nature of the base current and low-frequency noise – and without increasing the process complexity.

[0008] This invention fulfills this task by introducing a special doping profile into an epitaxially produced cap layer (cap doping). This doping profile allows achieving a minimal base-emitter capacity and best high-frequency properties, but also restricts the effect of a generation-active and recombination-active interface between the cap layer and the insulator

in the overlapping poly-silicon region in the interesting function range of the transistor, and improves the ideal nature of the base current.

[0009] Decisive for the good high-frequency properties is the base-side section in the cap layer of a preferable thickness between 20 nm and 70 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}.

[0010] On the emitter side, the cap layer is doped more highly. If the doping agent is of a conductivity type like the base layer, the doping agent concentration applied in the cap layer is preferably less than 5×10^{18} cm^{-3} in order to prevent tunnel currents.

[0011] The cap doping profile is preferably introduced by implantation in situ during the epitaxy procedure.

[0012] The characteristics of this invention are clear from the claims and also from the description and the drawings, where each characteristic – either individually or several characteristics in the form of sub-combinations – represent patentable designs, for which protection is demanded herein. Design examples are illustrated in the drawings and are explained in more detail in further text.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The drawings show:

Figure 1: A schematic illustration of the emitter zone of a bi-polar transistor manufactured with a single poly-silicon technology with an epitaxially deposited base,

Figure 2: A schematic illustration of the simulation region for the bi-polar transistor according to Fig. 1 (not in correct scale),

Figure 3: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 4: Transition frequency as a function of the collector current density for various doping profiles,

Figure 5: Graphs for various doping profiles,

Figure 6: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 7: Graphs for various doping profiles,

Figure 8: Transition frequency as a function of the collector current density for various doping profiles, and

Figure 9: A schematic illustration of a bi-polar transistor during the manufacturing process.

DETAILED DESCRIPTION OF THE INVENTION

[0014] The characteristics and effects of the cap doping profiles according to this invention are described by means of a two-dimensional element simulation on an npn SiGe HBT. The explanation can be applied to a pnp transistor accordingly.

[0015] Figure 6 shows characteristic examples for the vertical profiles (as proposed herein) in the cap layer 13 along a section line horizontal to the overlapping region. The doping agent concentration of the cap "profile p1" is growing in direction to the surface of the cap layer and reaches there its maximum concentration with about 9×10^{17} cm^{-3}, whereas the box-like profiles "p2" and "n3" are 10 nm wide and doped with 2×10^{18} cm^{-3}. The profiles p1 p2 are of a p conductivity type, profile n3 is of n-type. Figure 7 shows "Gummel" graphs to profiles p1, p2 and n3, when the characteristics of profile 1 from Fig. 5 were taken over for comparison. Figure 7 shows a clear improvement in the characteristics of the base current when cap doping is used as compared with the behavior of profile i. Dynamic calculations to these profiles lead to the results shown in Figure 8: Unlike the homogeneous dopings n1 and n2 with concentrations of 1×10^{18} cm^{-3} and 2×10^{17} cm^{-3}, profiles p1, p2 and n3 demonstrate no noticeable deterioration of transition frequencies in comparison with profile i. Decisive for the good high-frequency properties is the section in the cap layer of a preferable thickness of at least 20 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}. The results indicate that, in the example shown here, n-profiles and n-profiles in the cap layer can achieve comparable results.

[0016] In practice, the decision which doping type should be applied depends on the circumstance, e.g., of which type and density are the charges on the Si/insulator interface or in the insulator, or which manufacturing procedure can be used for the cap doping process. So, e.g., the proposed profiles can be introduced by implantation. However, this variant should be preferred only if the effects of point defects on the base profile can be controlled. Should the curing of the point defects lead to an increased diffusion of the base doping from the SiGe layer and, therefore, to an unacceptable deterioration of the electrical properties, other doping variants are required. For example, an in situ doping during the epitaxy process is possible. During this procedure, the type of the cap doping is co-determined by the safety and simplicity of the deposition process. The following text explains the manufacturing of a bi-polar transistor according to this invention on the example of an npn SiGe HBT. The revealed procedure can be applied to pnp transistors as well. In addition, according to this

invention it is also possible not to use an epitaxy process on the base layer and, instead, introduce the base profile by implantation before the epitaxial manufacturing of the cap layer.

[0017] As illustrated in Figure 9, structured regions consisting of a collector region 112 of the conductivity type II and an insulation region 113 (which surrounds the collector region 112) were produced on a monocrystal substrate layer 111 of the conductivity type I. If the emitter and the collector are, e.g., n-conductive, the base is of the p-type and vice versa. Various suitable insulation techniques are known such as LOCOS processes, spaced mesa arrangements or deep or flat trench insulation.

[0018] On the basis of a differential epitaxy process, a buffer layer 114, a SiGe layer with in-situ doping of the base layer 115 of the conductivity type I and a cap layer 116 are is applied on the entire surface.

[0019] While the buffer layer 114, the base layer 115 and the cap layer 116 grow – as monocrystal materials – on the silicon substrate, polycrystal layers 114/1, 115/1 and 116/1 arise over the insulation zone 113. After photolithographic masking, dry-etching techniques are applied to remove the epitaxy layer in those regions in which no transistors arise.

[0020] If a selective epitaxy process is used instead of differential epitaxy, where growth occurs exclusively on the silicon underground, the structuring of the epitaxy layer stack is eliminated.

[0021] In the following step, the silicon regions with an insulation layer 117 are exposed. This can be achieved by means of thermal oxidation and/or deposition. Layer stacks of dielectrica such as silicon oxide and silicon nitride can be applied. Besides that, the electrically conductive layer can be covered with a poly-silicon layer in order to maintain additional flexibility for the process at a later stage.

[0022] Essential from the point of view of the procedure according to this invention is the implementation of the cap doping profile in an epitaxially produced cap layer. There is a possibility to introduce similar profiles, as shown in Figure 6, in situ during the epitaxy process. Furthermore, a flat profile can be produced by implantation before or after the production of the insulation layer 117. In addition, various procedures for the diffusion of such profiles are also known. This can also be performed by means of an insulation layer highly enriched with the doping agent. A diffusion step can occur before or after further procedure steps. The use of diffusion-preventing ingredients in the collector, the base and the cap layer 116 such as carbon is especially useful if certain processes are used such as implantation, diffusion or thermal oxidation, which can cause an accelerated diffusion of the doping agents.

[0023] The transistor manufacturing process can now proceed with the structuring of a coating mask for the opening of the emitter window. In this step, the cover layers are removed in well-known etching procedures. In order to achieve good transistor properties, preferably wet-etching techniques should be used to expose the semiconductor surface.

[0024] The process continues with the deposition of an amorphous silicon layer for the creation of a poly-silicon emitter. This layer can be doped in situ by implantation during or immediately after the deposition.

[0025] The process then continues with conventional steps of structuring, implantation and passivation. The required high-temperature steps are taken to cure implantation defects and to form the poly-emitter. The manufacturing process is completed with the opening of the contact apertures for the emitter, the base and the collector and with a standard metallization of the transistor contacts.

[0026] This invention explains, on the basis of concrete design examples, a bi-polar transistor and a procedure for its manufacture. However, notice must be taken that this invention is not restricted to the particulars of the description of any particular design example, since, within the patent claims, changes and deviations are also subject to patent protection.

Bi-polar transistor and a procedure for its manufacture

The invention relates to a bi-polar transistor and a procedure for its manufacture.

The implementation of epitaxially manufactured silicon-germanium hetero-bi-polar transistors (SiGe HBT) and the [resulting] cost-reducing simplification of the technological processes have lately provided a new impetus for a further development of Si bi-polar transistors. In this respect, the combination of an epitaxially produced base with the process-simplifying possibilities of the single polysilicon technology offers an attractive direction of development.

In comparison with conventional base profiles produced by implantation or diffusion, silicon-germanium base layers made by epitaxy allow producing, simultaneously, smaller base widths and base layer resistance without unusable small current gains or high leakage currents. The technology allows implementation of a concentration of the active doping agent of up to 1 x 10^{20} cm^{-3}, as is described – for example – in *A. Schüppen, A. Gruhle, U. Erben, H. Kibbel und U. König: 90 GHz fmax SiGe-HBTs, DRC 94*, page IIA-2, 1994. However, in order to prevent leakage currents due to tunnel processes, a low-doped region is required between the high-concentration zones of the emitter and the base. As a matter of fact, if the base doping exceeds the value of 5 x 10^{18} cm^{-3}, and if the high concentration of the emitter reaches down to the base – as is usual with implanted base profiles – the consequence is the existence of unacceptably high tunnel currents. As opposed to implanted base profiles, the application of epitaxy allows, simultaneously and without any problems, the production of narrow base profiles and a low-doped region (cap layer).

Figure 1 illustrates the emitter zone of a SiGe HBT. This transistor design reflects typical characteristics of a single poly-silicon process. An SiGe base 12 and subsequently a cap layer 13 were deposited over a monocrystal collector zone 11. Figure 1 does not show a lateral insulation of the transistor zone. If semiconductor material grows both on the monocrystal substrate 11 and on the insulator zone – not shown in the picture – (i.e., differential epitaxy), it is possible to utilize the grown semiconductor layers as a connection between a contact on the insulation zone and the inner transistor. Such a connection should be designed with as low impedance as possible. This is why it would be advantageous if the epitaxial layer thickness could be set up independently from the base width. A poly-silicon or an α-silicon layer 15 is deposited on an insulation layer 14, in which emitter windows were etched by means of a wet-chemical etching process. During the deposition or subsequently, the α-silicon layer 15 obtains – by implantation – a doping of the emitter's conductivity type and serves as diffusion source for the emitter doping 16 in the monocrystal substrate. Insulator layer 14 is applied in order to prevent damage to cap layer 13 during the structuring of the polycrystal α-silicon layer 15 performed later. In the overlapping region 17 – a zone between the edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer 15, a layer sequence arises consisting of semiconductor material, insulator material and semiconductor material. Depending on the doping of the cap layer 13, the interfacial charges and the recombination properties of the surface as well as on the operation conditions of the transistor, this design can cause – analogous to a MOS capacity – an enhancement but also a depletion of mobile charge carriers on the

surface of the cap layer 13. With a forward-current base-emitter diode, this can affect both the ideal nature of the base current and the low-frequency noise properties. Under certain circumstances, generation currents and breakdown voltage in the non-conducting direction can be affected. The condition that – due to the tunnel [currents] danger – the doping agent concentration should not exceed the value of 5 x 10^{18} cm^{-3} leads to the question, by means of which procedure this zone should be suitably doped. The following text discusses the variants for SiGe HBT so far known: homogeneous n-doping or p-doping near the tunnel limit or quasi undoped zones (i-zones). *A. Chantre, M. Marty, J.L. Regolini, M. Mouis, J. de Pontcharra, D. Dutrtre, C. Morin, D. Gloria, S. Jouan, R. Pantel, M. Laurens and A. Monroy: A high performance low complexity SiGe HBT for BiCMOS integration, BCTM '98, 1998*, pages 93 – 96 uses a p-doping of about 5 x 10^{18} cm^{-3}. This results in a decisive disadvantage in that the thickness of the cap layer must be set up within a tolerance range of a few nanometers from the penetration depth of the doping agent diffusing from the poly-silicon emitter layer. Greater cap layer thickness values (which would be advantageous for a low-impedance connection between the inner base and a connector in the insulation zone) are not possible since it would negatively affect the effect of the germanium profile. *A. Gruhle, C. Mähner: Low l/f noise SiGe HBTs with application to low phase noise microwave oscillators, Electronics Letters, Vol. 33, No. 24, 1997*, pages 2050 – 2052 uses a cap layer 100 nm thick with an n-concentration of 1 - 2 x 10^{18} cm^{-3}. Although this variant eliminates the problem of the thickness tolerance, and avoids the danger of tunnel currents by reducing the doping agent concentration in the cap layer, it still does not take full advantage of the possibilities of reducing the base-emitter capacity.

This disadvantage can be eliminated by not doping the cap layer as is described, for example, in *B. Heinemann, F. Herzel and U. Zillmann: Influence of low doped emitter and collector regions on high-frequency performance SiGe-base HBTs, Solid-St. Electron, 1995*, Volume 38(6), pages 1183 - 1189. However, it can easily lead to a depletion of the aforementioned overlapping region 17. These connections are explained in further text by means of a two-dimension design element simulation.

Figure 2 shows the simplified transistor design used in the simulation. The electrical effect of the oxide semiconductor surface in the overlapping region is modeled by means of a positive surface charge density of 1 x 10^{11} cm^{-2} and a surface recombination speed of 1000 cm/s. Figure 3 illustrates vertical profiles along a section line horizontal to the overlapping region. The profiles show three doping variants in the cap layer 13 and a p-doped SiGe base 12 identical for all three cases. The following cap doping cases are compared: a quasi undoped cap layer 13 (profile i) and two homogeneous n-dopings (profile n1 with 1 x 10^{18} cm^{-3} and profile n2 with 2 x 10^{17} cm^{-3}). Figure 4 shows the transition frequency as a function of the collector current for various doping variants. Especially with small collector currents, an increase in transition frequency with a falling doping level in the cap layer 13 can be noticed. While profile i provides relatively best transition frequencies, it has, however, the disadvantage that the ideal nature of the base current (Figure 5) is noticeably affected in comparison with the other profiles.

The task of this invention is to indicate a bi-polar transistor and a procedure for its manufacture that eliminates the described disadvantages of conventional arrangements, in order to achieve especially minimal base-emitter capacities and best high-frequency properties without noticeably affecting the static properties of the bi-polar transistor with a low-doped cap layer -

above all the ideal nature of the base current and low-frequency noise – and without increasing the process complexity.

This invention fulfills this task by introducing a special doping profile into an epitaxially produced cap layer (cap doping). This doping profile allows achieving a minimal base-emitter capacity and best high-frequency properties, but also restricts the effect of a generation-active and recombination-active interface between the cap layer and the insulator in the overlapping poly-silicon region in the interesting function range of the transistor, and improves the ideal nature of the base current.

Decisive for the good high-frequency properties is the base-side section in the cap layer of a preferable thickness between 20 nm and 70 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}.

On the emitter side, the cap layer is doped more highly. If the doping agent is of a conductivity type like the base layer, the doping agent concentration applied in the cap layer is preferably less than 5×10^{18} cm^{-3} in order to prevent tunnel currents.

The cap doping profile is preferably introduced by implantation in situ during the epitaxy procedure.

The characteristics of this invention are clear from the claims and also from the description and the drawings, where each characteristic – either individually or several characteristics in the form of sub-combinations – represent patentable designs, for which protection is demanded herein. Design examples are illustrated in the drawings and are explained in more detail in further text.

The drawings show:

Figure 1: A schematic illustration of the emitter zone of a bi-polar transistor manufactured with a single poly-silicon technology with an epitaxially deposited base,

Figure 2: A schematic illustration of the simulation region for the bi-polar transistor according to Fig. 1 (not in correct scale),

Figure 3: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 4: Transition frequency as a function of the collector current density for various doping profiles,

Figure 5: Graphs for various doping profiles,

Figure 6: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 7: Graphs for various doping profiles,

Figure 8: Transition frequency as a function of the collector current density for various doping profiles, and

Figure 9: A schematic illustration of a bi-polar transistor during the manufacturing process.

The characteristics and effects of the cap doping profiles according to this invention are described by means of a two-dimensional element simulation on an npn SiGe HBT. The explanation can be applied to a pnp transistor accordingly.

Figure 6 shows characteristic examples for the vertical profiles (as proposed herein) in the cap layer 13 along a section line horizontal to the overlapping region. The [doping agent concentration of the] cap "profile p1" is growing in direction to the surface of the cap layer and reaches there its maximum concentration with about 9×10^{17} cm^{-3}, whereas the box-like profiles "p2" and "n3" are 10 nm wide and doped with 2×10^{18} cm^{-3}. The profiles p1 p2 are of a p conductivity type, profile n3 is of n-type. Figure 7 shows "Gummel" graphs to profiles p1, p2 and n3, when the characteristics of profile 1 from Fig. 5 were taken over for comparison. Figure 7 shows a clear improvement in the characteristics of the base current when cap doping is used as compared with the behavior of profile i. Dynamic calculations to these profiles lead to the results shown in Figure 8: Unlike the homogeneous dopings n1 and n2 with concentrations of 1×10^{18} cm^{-3} and 2×10^{17} cm^{-3}, profiles p1, p2 and n3 demonstrate no noticeable deterioration of transition frequencies in comparison with profile i. Decisive for the good high-frequency properties is the section in the cap layer of a preferable thickness of at least 20 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}. The results indicate that, in the example shown here, n-profiles and n-profiles in the cap layer can achieve comparable results.

In practice, the decision which doping type should be applied depends on the circumstance, e.g., of which type and density are the charges on the Si/insulator interface or in the insulator, or which manufacturing procedure can be used for the cap doping process. So, e.g., the proposed profiles can be introduced by implantation. However, this variant should be preferred only if the effects of point defects on the base profile can be controlled. Should the curing of the point defects lead to an increased diffusion of the base doping from the SiGe layer and, therefore, to an unacceptable deterioration of the electrical properties, other doping variants are required. For example, an in situ doping during the epitaxy process is possible. During this procedure, the type of the cap doping is co-determined by the safety and simplicity of the deposition process. The following text explains the manufacturing of a bi-polar transistor according to this invention on the example of an npn SiGe HBT. The revealed procedure can be applied to pnp transistors as well. In addition, according to this invention it is also possible not to use an epitaxy process on the base layer and, instead, introduce the base profile by implantation before the epitaxial manufacturing of the cap layer.

As illustrated in Figure 9, structured regions consisting of a collector region 112 of the conductivity type II and an insulation region 113 (which surrounds the collector region 112) were produced on a monocrystal substrate layer 111 of the conductivity type I. If the emitter and

the collector are, e.g., n-conductive, the base is of the p-type and vice versa. Various suitable insulation techniques are known such as LOCOS processes, spaced mesa arrangements or deep or flat trench insulation.

On the basis of a differential epitaxy process, a buffer layer 114, a SiGe layer with in-situ doping of the base layer 115 of the conductivity type I and a cap layer 116 are is applied on the entire surface.

While the buffer layer 114, the base layer 115 and the cap layer 116 grow – as monocrystal materials – on the silicon substrate, polycrystal layers 114/1, 115/1 and 116/1 arise over the insulation zone 113. After photolithographic masking, dry-etching techniques are applied to remove the epitaxy layer in those regions in which no transistors arise.

If a selective epitaxy process is used instead of differential epitaxy, where growth occurs exclusively on the silicon underground, the structuring of the epitaxy layer stack is eliminated.

In the following step, the silicon regions with an insulation layer 117 are exposed. This can be achieved by means of thermal oxidation and/or deposition. Layer stacks of dielectrica such as silicon oxide and silicon nitride can be applied. Besides that, the electrically conductive layer can be covered with a poly-silicon layer in order to maintain additional flexibility for the process at a later stage.

Essential from the point of view of the procedure according to this invention is the implementation of the cap doping profile in an epitaxially produced cap layer. There is a possibility to introduce similar profiles, as shown in Figure 6, in situ during the epitaxy process. Furthermore, a flat profile can be produced by implantation before or after the production of the insulation layer 117. In addition, various procedures for the diffusion of such profiles are also known. This can also be performed by means of an insulation layer highly enriched with the doping agent. A diffusion step can occur before or after further procedure steps. The use of diffusion-preventing ingredients in the collector, the base and the cap layer 116 such as carbon is especially useful if certain processes are used such as implantation, diffusion or thermal oxidation, which can cause an accelerated diffusion of the doping agents.

The transistor manufacturing process can now proceed with the structuring of a coating mask for the opening of the emitter window. In this step, the cover layers are removed in well-known etching procedures. In order to achieve good transistor properties, preferably wet-etching techniques should be used to expose the semiconductor surface.

The process continues with the deposition of an amorphous silicon layer for the creation of a poly-silicon emitter. This layer can be doped in situ by implantation during or immediately after the deposition.

The process then continues with conventional steps of structuring, implantation and passivation. The required high-temperature steps are taken to cure implantation defects and to form the poly-emitter. The manufacturing process is completed with the opening of the contact

apertures for the emitter, the base and the collector and with a standard metallization of the transistor contacts.

This invention explains, on the basis of concrete design examples, a bi-polar transistor and a procedure for its manufacture. However, notice must be taken that this invention is not restricted to the particulars of the description of any particular design example, since, within the patent claims, changes and deviations are also subject to patent protection.

Patent claims

1. A procedure for the manufacture of a bi-polar transistor, during which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and, by means of epitaxy, a cap layer (116) are produced over the collector zone (112), an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that** a doping profile is introduced into the cap layer (116), and the profile is low-doped on the base side and highly doped on the emitter side.

2. A procedure according to claim 1, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed values of 5×10^{16} cm^{-3}.

3. A procedure according to claims 1 or 2, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed the thickness of 70 nm.

4. A procedure according to one or several of the preceding claims, **characterized in that** the base-side lower doping concentration of the cap layer (116) of a layer thickness of 20 nm does not exceed values of 5×10^{16} cm^{-3}.

5. A procedure according to one or several of the preceding claims, **characterized in that** the emitter-side high doping concentration of the cap layer (116) does not exceed values of
5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (115).

6. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by implantation.

7. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced in situ during the epitaxy process.

8. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by diffusion from the insulation layer (117) that had been highly enriched with the doping agent.

9. A procedure according to one or several of the preceding claims, **characterized in that** the base is produced by epitaxy.

10. A procedure according to one or several of the preceding claims, **characterized in that** the base layer (115) is implemented as an SiGe layer by epitaxy.

11. A procedure according to one or several of the preceding claims, **characterized in that** a diffusion-preventing ingredient is introduced into the collector zone (112), the base layer (115) and/or the emitter zone.

12. A procedure according to one or several of the preceding claims, **characterized in that** carbon is introduced as a diffusion-preventing ingredient.

13. A procedure according to one or several of the preceding claims, **characterized in that** boron in a concentration of over 5×10^{18} cm^{-3} is introduced into the base layer (115).

14. A bi-polar transistor, in which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and, by means of epitaxy, a cap layer (116) are produced over the collector zone (112), an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that** a doping profile is introduced into the cap layer (116), and the profile is low-doped on the base side and highly doped on the emitter side.

15. A bi-polar transistor according to claim 14, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed values of 5×10^{16} cm^{-3}.

16. A bi-polar transistor according to claims 14 or 15, **characterized in that** the base-side lower doping concentration of the cap layer (116) of a layer thickness of at least 20 nm does not exceed values of 5×10^{16} cm^{-3}.

17. A bi-polar transistor according to one or several of claims 14 to 16, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed the thickness of 70 nm.

18. A bi-polar transistor according to one or several of claims 14 to 17, **characterized in that** the emitter-side high doping concentration of the cap layer (116) does not exceed values of 5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (115).

Summary

The task of this invention is to indicate a bi-polar transistor and a procedure for its manufacture that achieves minimal base-emitter capacities and best high-frequency properties without noticeably affecting the static properties of the bi-polar transistor with a low-doped cap layer - above all the ideal nature of the base current and low-frequency noise – and without increasing the process complexity.

This invention fulfills this task by introducing a special doping profile into an epitaxially produced cap layer (cap doping). This doping profile allows achieving a minimal base-emitter capacity and best high-frequency properties, but also restricts the effect of a generation-active and recombination-active interface between the cap layer and the insulator in the overlapping poly-silicon region in the interesting function range of the transistor, and improves the ideal nature of the base current.

Decisive for the good high-frequency properties is the base-side section in the cap layer of a preferable thickness between 20 nm and 70 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}.

Figures 1 to 9:

Polysilizium = poly-silicon
SiGe-Basis = SiGe base
Kollektor = collector
Cap-Schicht = cap layer
Konzentration = concentration
Profil = profile
Abstand zur Si/SiO_2 Grenzfläche = distance to Si/SiO_2 surface
Transitfrequenz = transition frequency
Kollektorstrom = collector current
Basis = base
Spannung = voltage

Bi-polar transistor and a procedure for its manufacture

The invention relates to a bi-polar transistor and a procedure for its manufacture.

The implementation of epitaxially manufactured silicon-germanium hetero-bi-polar transistors (SiGe HBT) and the [resulting] cost-reducing simplification of the technological processes have lately provided a new impetus for a further development of Si bi-polar transistors. In this respect, the combination of an epitaxially produced base with the process-simplifying possibilities of the single polysilicon technology offers an attractive direction of development.

In comparison with conventional base profiles produced by implantation or diffusion, silicon-germanium base layers made by epitaxy allow producing, simultaneously, smaller base widths and base layer resistance without unusable small current gains or high leakage currents. The technology allows implementation of a concentration of the active doping agent of up to 1 x 10^{20} cm^{-3}, as is described – for example – in *A. Schüppen, A. Gruhle, U. Erben, H. Kibbel und U. König: 90 GHz fmax SiGe-HBTs, DRC 94*, page IIA-2, 1994. However, in order to prevent leakage currents due to tunnel processes, a low-doped region is required between the high-concentration zones of the emitter and the base. As a matter of fact, if the base doping exceeds the value of 5 x 10^{18} cm^{-3}, and if the high concentration of the emitter reaches down to the base – as is usual with implanted base profiles – the consequence is the existence of unacceptably high tunnel currents. As opposed to implanted base profiles, the application of epitaxy allows, simultaneously and without any problems, the production of narrow base profiles and a low-doped region (cap layer).

Figure 1 illustrates the emitter zone of a SiGe HBT. This transistor design reflects typical characteristics of a single poly-silicon process. An SiGe base 12 and subsequently a cap layer 13 were deposited over a monocrystal collector zone 11. Figure 1 does not show a lateral insulation of the transistor zone. If semiconductor material grows both on the monocrystal substrate 11 and on the insulator zone – not shown in the picture – (i.e., differential epitaxy), it is possible to utilize the grown semiconductor layers as a connection between a contact on the insulation zone and the inner transistor. Such a connection should be designed with as low impedance as possible. This is why it would be advantageous if the epitaxial layer thickness could be set up independently from the base width. A poly-silicon or an α-silicon layer 15 is deposited on an insulation layer 14, in which emitter windows were etched by means of a wet-chemical etching process. During the deposition or subsequently, the α-silicon layer 15 obtains – by implantation – a doping of the emitter's conductivity type and serves as diffusion source for the emitter doping 16 in the monocrystal substrate. Insulator layer 14 is applied in order to prevent damage to cap layer 13 during the structuring of the polycrystal α-silicon layer 15 performed later. In the overlapping region 17 – a zone between the edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer 15, a layer sequence arises consisting of semiconductor material, insulator material and semiconductor material. Depending on the doping of the cap layer 13, the interfacial charges and the recombination properties of the surface as well as on the operation conditions of the transistor, this design can cause – analogous to a MOS capacity – an enhancement but also a depletion of mobile charge carriers on the

surface of the cap layer 13. With a forward-current base-emitter diode, this can affect both the ideal nature of the base current and the low-frequency noise properties. Under certain circumstances, generation currents and breakdown voltage in the non-conducting direction can be affected. The condition that – due to the tunnel [currents] danger – the doping agent concentration should not exceed the value of 5 x 10^{18} cm^{-3} leads to the question, by means of which procedure this zone should be suitably doped. The following text discusses the variants for SiGe HBT so far known: homogeneous n-doping or p-doping near the tunnel limit or quasi undoped zones (i-zones). *A. Chantre, M. Marty, J.L. Regolini, M. Mouis, J. de Pontcharra, D. Dutrtre, C. Morin, D. Gloria, S. Jouan, R. Pantel, M. Laurens and A. Monroy: A high performance low complexity SiGe HBT for BiCMOS integration, BCTM '98, 1998*, pages 93 – 96 uses a p-doping of about 5 x 10^{18} cm^{-3}. This results in a decisive disadvantage in that the thickness of the cap layer must be set up within a tolerance range of a few nanometers from the penetration depth of the doping agent diffusing from the poly-silicon emitter layer. Greater cap layer thickness values (which would be advantageous for a low-impedance connection between the inner base and a connector in the insulation zone) are not possible since it would negatively affect the effect of the germanium profile. *A. Gruhle, C. Mähner: Low l/f noise SiGe HBTs with application to low phase noise microwave oscillators, Electronics Letters, Vol. 33, No. 24, 1997*, pages 2050 – 2052 uses a cap layer 100 nm thick with an n-concentration of 1 - 2 x 10^{18} cm^{-3}. EP-A-0 795 899 indicates similar conditions, where preferably a cap layer of a thickness of 70 nm with a n-doping concentration of 2 x 10^{18} cm^{-3} is used. Although this variant eliminates the problem of the thickness tolerance, and avoids the danger of tunnel currents by reducing the doping agent concentration in the cap layer, it still does not take full advantage of the possibilities of reducing the base-emitter capacity.

This disadvantage can be eliminated by not doping the cap layer as is described, for example, in *B. Heinemann, F. Herzel and U. Zillmann: Influence of low doped emitter and collector regions on high-frequency performance SiGe-base HBTs, Solid-St. Electron, 1995*, Volume 38(6), pages 1183 - 1189. However, it can easily lead to a depletion of the aforementioned overlapping region 17. These connections are explained in further text by means of a two-dimension design element simulation.

Figure 2 shows the simplified transistor design used in the simulation. The electrical effect of the oxide semiconductor surface in the overlapping region is modeled by means of a positive surface charge density of 1 x 10^{11} cm^{-2} and a surface recombination speed of 1000 cm/s. Figure 3 illustrates vertical profiles along a section line horizontal to the overlapping region. The profiles show three doping variants in the cap layer 13 and a p-doped SiGe base 12 identical for all three cases. The following cap doping cases are compared: a quasi undoped cap layer 13 (profile i) and two homogeneous n-dopings (profile n1 with 1 x 10^{18} cm^{-3} and profile n2 with 2 x 10^{17} cm^{-3}). Figure 4 shows the transition frequency as a function of the collector current for various doping variants. Especially with small collector currents, an increase in transition frequency with a falling doping level in the cap layer 13 can be noticed. While profile i provides relatively best transition frequencies, it has, however, the disadvantage that the ideal nature of the base current (Figure 5) is noticeably affected in comparison with the other profiles.

The task of this invention is to indicate a bi-polar transistor and a procedure for its manufacture that eliminates the described disadvantages of conventional arrangements, in order

to achieve especially minimal base-emitter capacities and best high-frequency properties without noticeably affecting the static properties of the bi-polar transistor with a low-doped cap layer - above all the ideal nature of the base current and low-frequency noise – and without increasing the process complexity.

This invention fulfills this task by introducing a special doping profile into an epitaxially produced cap layer (cap doping). This doping profile allows achieving a minimal base-emitter capacity and best high-frequency properties, but also restricts the effect of a generation-active and recombination-active interface between the cap layer and the insulator in the overlapping poly-silicon region in the interesting function range of the transistor, and improves the ideal nature of the base current.

Decisive for the good high-frequency properties is the base-side section in the cap layer of a preferable thickness between 20 nm and 70 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}.

On the emitter side, the cap layer is doped more highly. If the doping agent is of a conductivity type like the base layer, the doping agent concentration applied in the cap layer is preferably less than 5×10^{18} cm^{-3} in order to prevent tunnel currents.

The cap doping profile is preferably introduced by implantation in situ during the epitaxy procedure.

The characteristics of this invention are clear from the claims and also from the description and the drawings, where each characteristic – either individually or several characteristics in the form of sub-combinations – represent patentable designs, for which protection is demanded herein. Design examples are illustrated in the drawings and are explained in more detail in further text.

The drawings show:

Figure 1: A schematic illustration of the emitter zone of a bi-polar transistor manufactured with a single poly-silicon technology with an epitaxially deposited base,

Figure 2: A schematic illustration of the simulation region for the bi-polar transistor according to Fig. 1 (not in correct scale),

Figure 3: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 4: Transition frequency as a function of the collector current density for various doping profiles,

Figure 5: Graphs for various doping profiles,

Figure 6: Vertical doping profiles under the overlapping region for various cap doping

levels,

Figure 7: Graphs for various doping profiles,

Figure 8: Transition frequency as a function of the collector current density for various doping profiles, and

Figure 9: A schematic illustration of a bi-polar transistor during the manufacturing process.

The characteristics and effects of the cap doping profiles according to this invention are described by means of a two-dimensional element simulation on an npn SiGe HBT. The explanation can be applied to a pnp transistor accordingly.

Figure 6 shows characteristic examples for the vertical profiles (as proposed herein) in the cap layer 13 along a section line horizontal to the overlapping region. The [doping agent concentration of the] cap "profile p1" is growing in direction to the surface of the cap layer and reaches there its maximum concentration with about 9×10^{17} cm^{-3}, whereas the box-like profiles "p2" and "n3" are 10 nm wide and doped with 2×10^{18} cm^{-3}. The profiles p1 p2 are of a p conductivity type, profile n3 is of n-type. Figure 7 shows "Gummel" graphs to profiles p1, p2 and n3, when the characteristics of profile 1 from Fig. 5 were taken over for comparison. Figure 7 shows a clear improvement in the characteristics of the base current when cap doping is used as compared with the behavior of profile i. Dynamic calculations to these profiles lead to the results shown in Figure 8: Unlike the homogeneous dopings n1 and n2 with concentrations of 1×10^{18} cm^{-3} and 2×10^{17} cm^{-3}, profiles p1, p2 and n3 demonstrate no noticeable deterioration of transition frequencies in comparison with profile i. Decisive for the good high-frequency properties is the section in the cap layer of a preferable thickness of at least 20 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}. The results indicate that, in the example shown here, n-profiles and n-profiles in the cap layer can achieve comparable results.

In practice, the decision which doping type should be applied depends on the circumstance, e.g., of which type and density are the charges on the Si/insulator interface or in the insulator, or which manufacturing procedure can be used for the cap doping process. So, e.g., the proposed profiles can be introduced by implantation. However, this variant should be preferred only if the effects of point defects on the base profile can be controlled. Should the curing of the point defects lead to an increased diffusion of the base doping from the SiGe layer and, therefore, to an unacceptable deterioration of the electrical properties, other doping variants are required. For example, an in situ doping during the epitaxy process is possible. During this procedure, the type of the cap doping is co-determined by the safety and simplicity of the deposition process. The following text explains the manufacturing of a bi-polar transistor according to this invention on the example of an npn SiGe HBT. The revealed procedure can be applied to pnp transistors as well. In addition, according to this invention it is also possible not to use an epitaxy process on the base layer and, instead, introduce the base profile by implantation before the epitaxial manufacturing of the cap layer.

As illustrated in Figure 9, structured regions consisting of a collector region 112 of the conductivity type II and an insulation region 113 (which surrounds the collector region 112) were produced on a monocrystal substrate layer 111 of the conductivity type I. If the emitter and the collector are, e.g., n-conductive, the base is of the p-type and vice versa. Various suitable insulation techniques are known such as LOCOS processes, spaced mesa arrangements or deep or flat trench insulation.

On the basis of a differential epitaxy process, a buffer layer 114, a SiGe layer with in-situ doping of the base layer 115 of the conductivity type I and a cap layer 116 are is applied on the entire surface.

While the buffer layer 114, the base layer 115 and the cap layer 116 grow – as monocrystal materials – on the silicon substrate, polycrystal layers 114/1, 115/1 and 116/1 arise over the insulation zone 113. After photolithographic masking, dry-etching techniques are applied to remove the epitaxy layer in those regions in which no transistors arise.

If a selective epitaxy process is used instead of differential epitaxy, where growth occurs exclusively on the silicon underground, the structuring of the epitaxy layer stack is eliminated.

In the following step, the silicon regions with an insulation layer 117 are exposed. This can be achieved by means of thermal oxidation and/or deposition. Layer stacks of dielectrica such as silicon oxide and silicon nitride can be applied. Besides that, the electrically conductive layer can be covered with a poly-silicon layer in order to maintain additional flexibility for the process at a later stage.

Essential from the point of view of the procedure according to this invention is the implementation of the cap doping profile in an epitaxially produced cap layer. There is a possibility to introduce similar profiles, as shown in Figure 6, in situ during the epitaxy process. Furthermore, a flat profile can be produced by implantation before or after the production of the insulation layer 117. In addition, various procedures for the diffusion of such profiles are also known. This can also be performed by means of an insulation layer highly enriched with the doping agent. A diffusion step can occur before or after further procedure steps. The use of diffusion-preventing ingredients in the collector, the base and the cap layer 116 such as carbon is especially useful if certain processes are used such as implantation, diffusion or thermal oxidation, which can cause an accelerated diffusion of the doping agents.

The transistor manufacturing process can now proceed with the structuring of a coating mask for the opening of the emitter window. In this step, the cover layers are removed in well-known etching procedures. In order to achieve good transistor properties, preferably wet-etching techniques should be used to expose the semiconductor surface.

The process continues with the deposition of an amorphous silicon layer for the creation of a poly-silicon emitter. This layer can be doped in situ by implantation during or immediately after the deposition.

The process then continues with conventional steps of structuring, implantation and passivation. The required high-temperature steps are taken to cure implantation defects and to form the poly-emitter. The manufacturing process is completed with the opening of the contact apertures for the emitter, the base and the collector and with a standard metallization of the transistor contacts.

This invention explains, on the basis of concrete design examples, a bi-polar transistor and a procedure for its manufacture. However, notice must be taken that this invention is not restricted to the particulars of the description of any particular design example, since, within the patent claims, changes and deviations are also subject to patent protection.

Patent claims

1. A procedure for the manufacture of a bi-polar transistor, during which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and, by means of epitaxy, a cap layer (116) are produced over the collector zone (112) – where an interposed buffer layer (114) can be deposited -, an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that** – before the diffusion from the emitter-doping agent source - a doping profile is introduced into the cap layer (116), and the profile is low-doped on the base side and highly doped on the emitter side.

2. A procedure according to claim 1, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed values of 5×10^{16} cm^{-3}.

3. A procedure according to claims 1 or 2, **characterized in that** the cap layer (116) is of a thickness between 20 nm and 70 nm.

4. A procedure according to one or several of the preceding claims, **characterized in that** the emitter-side high doping concentration of the cap layer (116) does not exceed values of 5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (115).

5. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by implantation.

6. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced in situ during the epitaxy process.

7. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by diffusion from the insulation layer (117) that had been highly enriched with the doping agent.

8. A bi-polar transistor, in which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and – where a buffer layer (114) can be interposed -, by means of epitaxy, a cap layer (116) are produced over the collector zone (112), an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that,** in the overlapping region (17) – the region between the edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer (15) – the cap layer (13/116) contains a doping profile, and the profile is low-doped on the base side and highly doped on the emitter side.

9. A bi-polar transistor according to claim 8, **characterized in that** the base-side lower doping concentration of the cap layer (13/116) does not exceed values of 5×10^{16} cm^{-3}.

10. A bi-polar transistor according to one or several of claims 8 to 9, **characterized in that** the cap layer (13/116) is of a thickness between 20 nm and 70 nm.

11. A bi-polar transistor according to one or several of claims 8 to 10, **characterized in that** the emitter-side high doping concentration of the cap layer (13/116) does not exceed values of 5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (12,115).

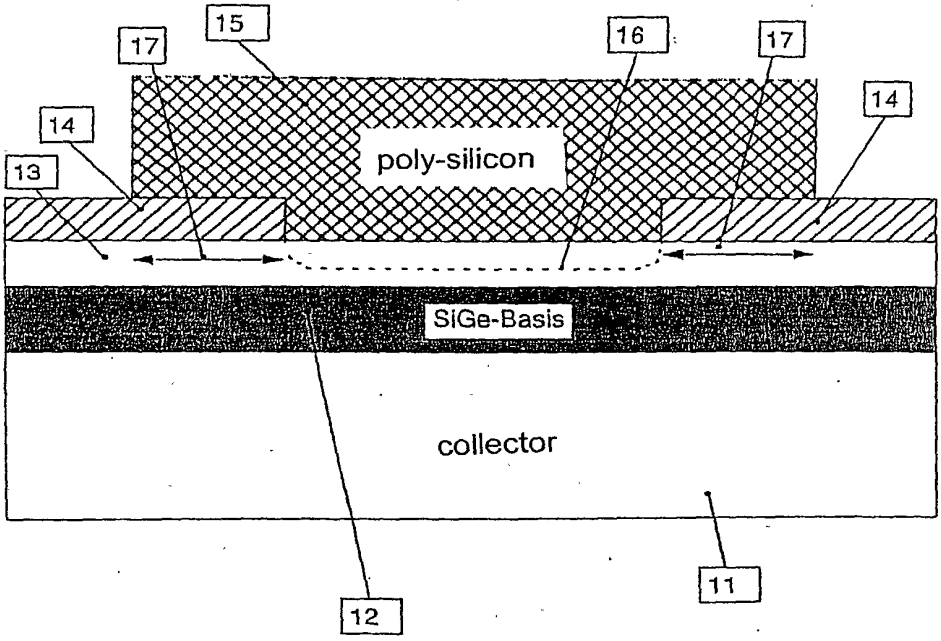
15
17
16
17
14
14
13
poly-silicon
SiGe-Basis
collector
12
11

Fig. 1

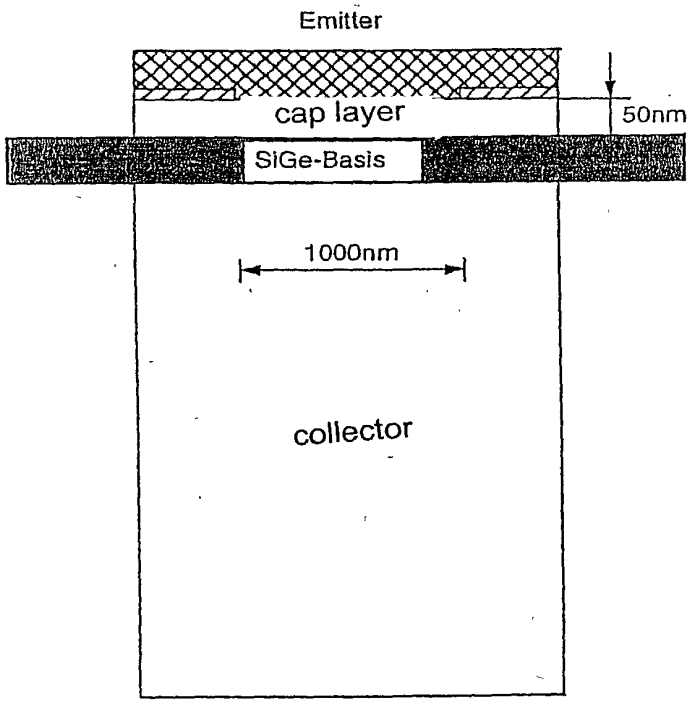
Emitter
cap layer
50nm
SiGe-Basis
1000nm
collector

Fig. 2

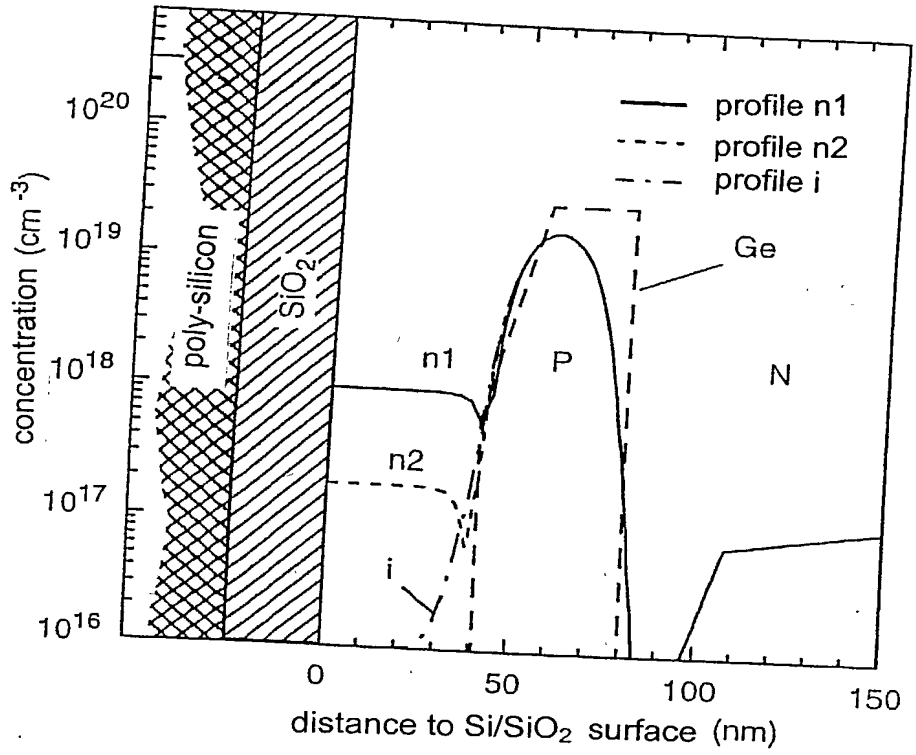
profile n1
profile n2
profile i
Ge
poly-silicon
SiO2
n1
P
N
n2
i
concentration (cm-3)
10^20
10^19
10^18
10^17
10^16
0
50
100
150
distance to Si/SiO2 surface (nm)

Fig. 3

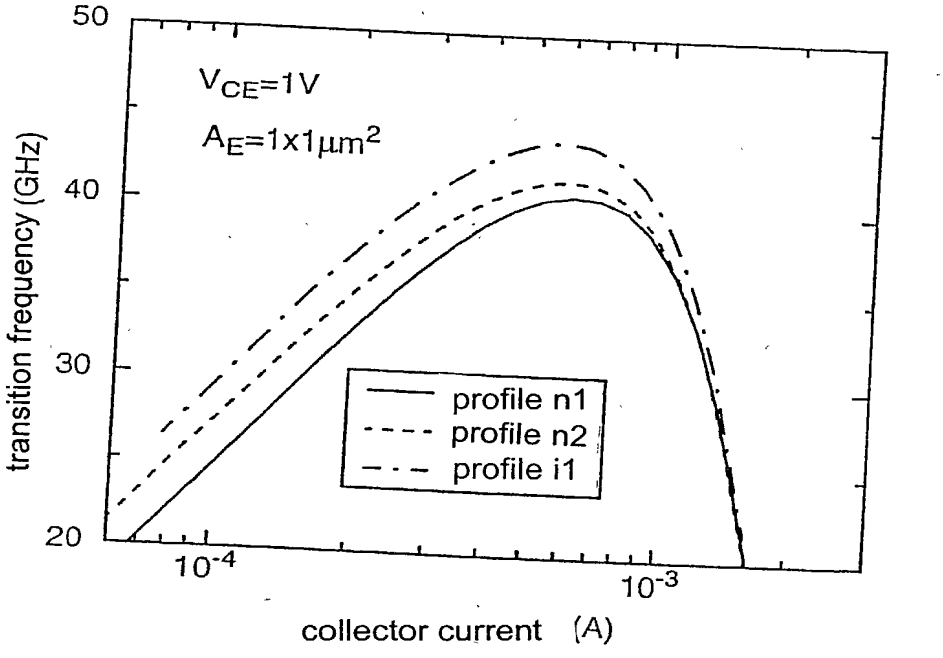
VCE=1V
AE=1x1μm2
profile n1
profile n2
profile i1
transition frequency (GHz)
50
40
30
20
10-4
10-3
collector current (A)

Fig. 4

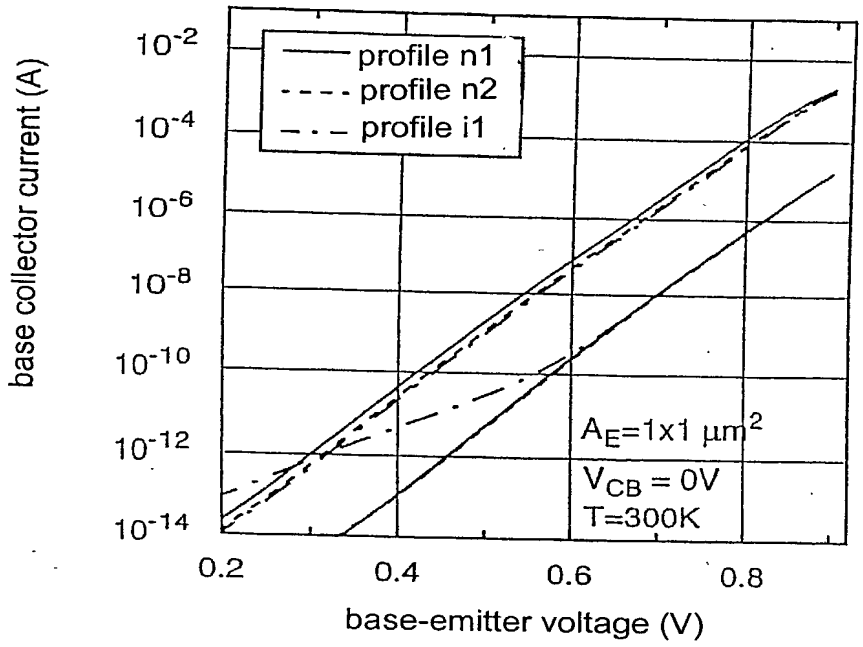
base collector current (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
10^{-14}
profile n1
profile n2
profile i1
A_E=1x1 µm^2
V_{CB} = 0V
T=300K
0.2
0.4
0.6
0.8
base-emitter voltage (V)

Fig. 5

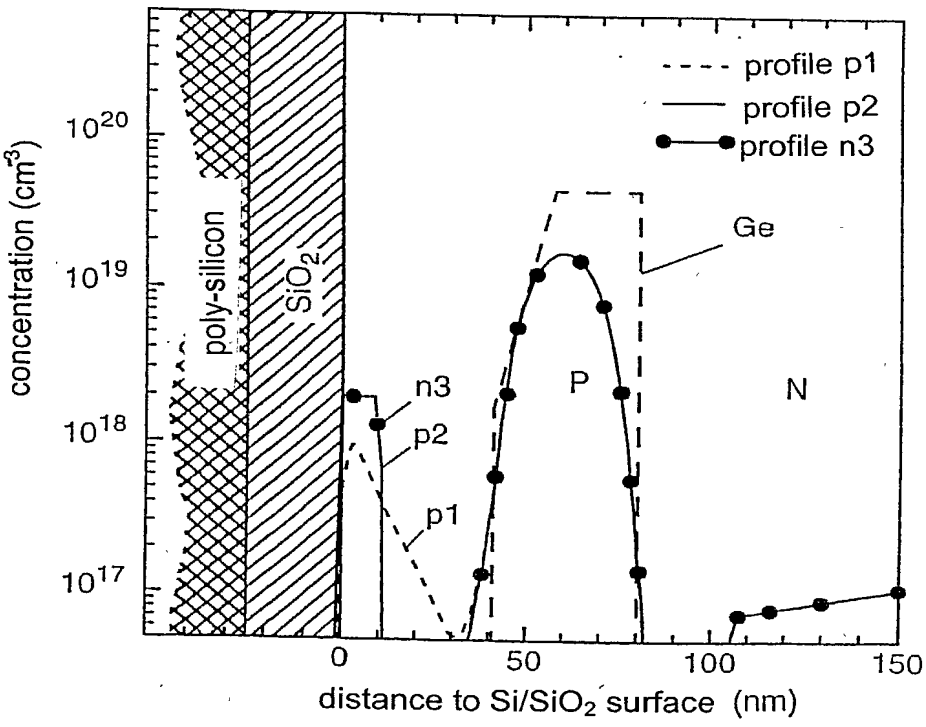
concentration (cm^3)
10^{20}
10^{19}
10^{18}
10^{17}
poly-silicon
SiO_2
profile p1
profile p2
profile n3
Ge
n3
p2
p1
P
N
0
50
100
150
distance to Si/SiO_2 surface (nm)

Fig. 6

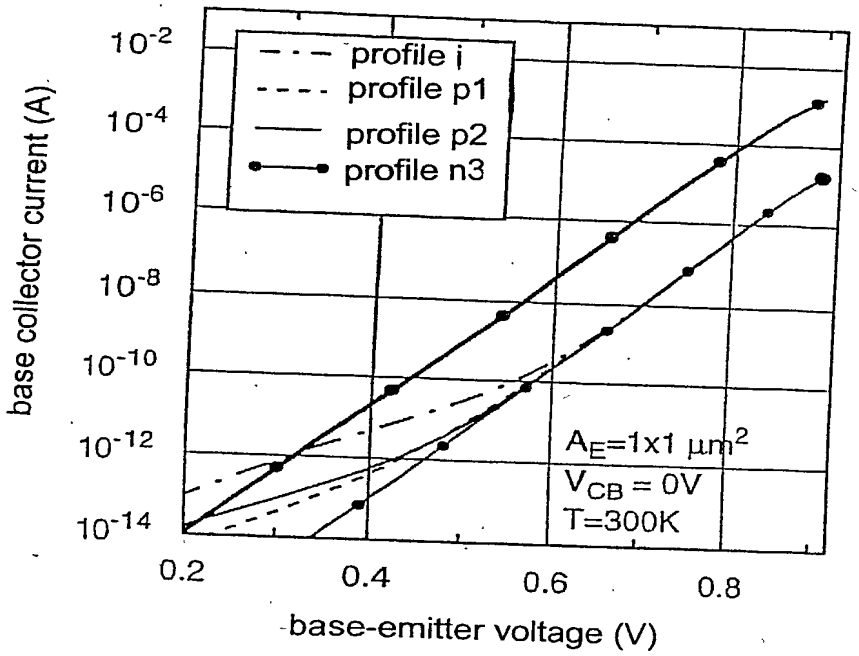
base collector current (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
10^{-14}
profile i
profile p1
profile p2
profile n3
A_E=1x1 μm^2
V_{CB} = 0V
T=300K
0.2
0.4
0.6
0.8
base-emitter voltage (V)

Fig. 7

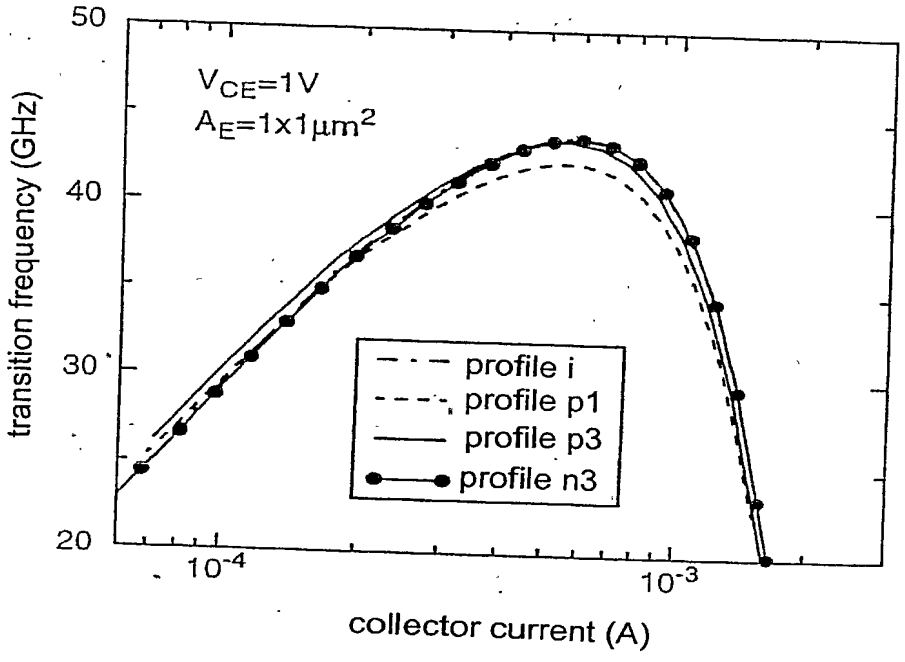
transition frequency (GHz)
50
40
30
20
V_{CE}=1V
A_E=1x1μm^2
profile i
profile p1
profile p3
profile n3
10^{-4}
10^{-3}
collector current (A)

Fig. 8

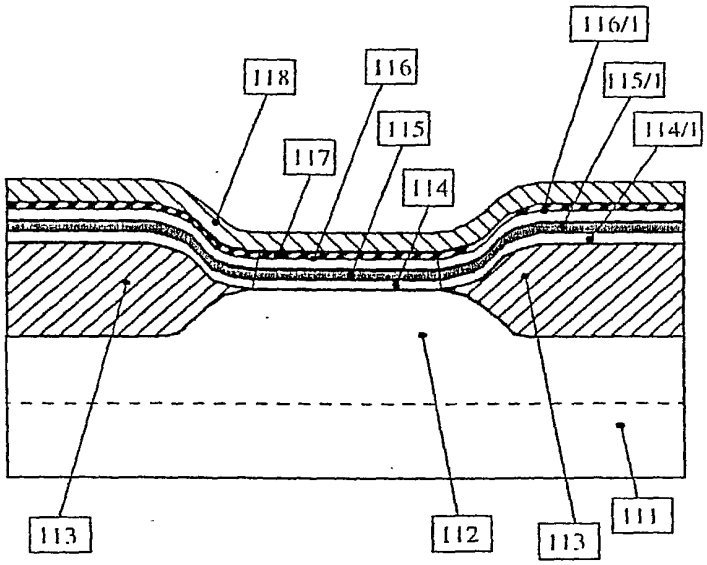

Fig. 9

Practitioner's Docket No. 7040-30 ***PATENT***

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is for a national stage of PCT application.

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am an original, first and joint inventor of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

BIPOLAR TRANSISTOR AND METHOD FOR PRODUCING SAME

SPECIFICATION IDENTIFICATION

The specification was described and claimed in PCT International Application No. PCT/DE99/03961 filed on December 8, 1999 and was amended under PCT Article 19 on November 15, 2000.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, Section 1.56, and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent.

PRIORITY CLAIM (35 U.S.C. Section 119(a)-(d))

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international

application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

Such applications have been filed as follows.

PRIOR FOREIGN APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. SECTION 119(a)-(d)

COUNTRY	APPLICATION NUMBER	DATE OF FILING DAY, MONTH, YEAR	PRIORITY CLAIMED UNDER 35 U.S.C. SECTION 119
Germany	198 57 640.4	14 December 1998	yes

POWER OF ATTORNEY

I hereby appoint the following practitioner(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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